

**Amendments to the Claims:**

The below listing of claims will replace all prior versions, and listings, of claims in the application.

**Listing of Claims**

1. (Currently amended) A voltage-controlled oscillator circuit connected to supply and reference voltages for radio frequency operation, comprising:

at least one inductor;

at least one varactor connected in parallel with the at least one inductor;

a pair of p-channel MOS transistors connected across the at least one varactor, each p-channel transistor having source, drain, and gate terminals, wherein the drain terminal of the first of the pair of p-channel MOS transistors is connected to the gate terminal of the second of the pair of p-channel MOS transistors and the drain terminal of the second of the pair of MOS transistors being is connected to the gate terminal of the first of the pair of MOS transistors; and

biasing means for providing a biasing current to the voltage-controlled oscillator circuit and for substantially widening the tuning range thereof, the biasing means being configured according to ~~one of~~ a biasing n-channel MOS transistor connected to the supply voltage and biasing self-biasing p-channel MOS transistor connected to the reference voltage,

wherein the biasing means is connected to the pair of p-channel MOS transistors and the at least one inductor.

2. (Original) The voltage-controlled oscillator circuit of claim 1, wherein when the biasing means is configured according to the biasing n-channel MOS transistor connected to the supply voltage, the biasing n-channel MOS transistor having source, drain, and gate terminals, the drain terminal of the biasing n-channel MOS transistor is connected to the supply voltage.

3. (Original) The voltage-controlled oscillator circuit of claim 2, wherein the gate terminal of the biasing n-channel MOS transistor is connected to a biasing voltage.
4. (Original) The voltage-controlled oscillator circuit of claim 3, wherein the source terminal of the biasing n-channel MOS transistor is connected to the source terminals of the pair of p-channel MOS transistors.
5. (Original) The voltage-controlled oscillator circuit of claim 4, wherein the at least one inductor is configured according to a pair of first and second inductors connected in series and the connection therebetween is connected to the reference voltage.
6. (Original) The voltage-controlled oscillator circuit of claim 1, wherein when the biasing means is configured according to the biasing p-channel MOS transistor connected to the reference voltage, the biasing p-channel MOS transistor having source, drain and gate terminals, the drain terminal of the biasing p-channel MOS transistor is connected to the reference voltage.
7. (Original) The voltage-controlled oscillator circuit of claim 6, wherein the gate and drain terminals of the biasing p-channel MOS transistor are connected.
8. (Original) The voltage-controlled oscillator circuit of claim 7, wherein the at least one inductor is configured according to a pair of first and second inductors connected in series.
9. (Original) The voltage-controlled oscillator circuit of claim 8, wherein the source terminal of the biasing p-channel MOS transistor is connected to the interconnection between the pair of first and second inductors.
10. (Original) The voltage-controlled oscillator circuit of claim 9, wherein the source terminals of the pair of p-channel MOS transistors are connected to the supply voltage
- 11-18. (Cancelled)

19. (Currently amended) A method for configuring a voltage-controlled oscillator circuit connected to supply and reference voltages for radio frequency operation, the method comprising the steps of:

providing at least one inductor;

connecting at least one varactor in parallel with the at least one inductor;

connecting a pair of p-channel MOS transistors across the at least one varactor, each p-channel transistor having source, drain, and gate terminals, wherein the drain terminal of the first of the pair of p-channel MOS transistors is connected to the gate terminal of the second of the pair of p-channel MOS transistors and the drain terminal of the second of the pair of p-channel MOS transistors ~~being~~ is connected to the gate terminal of the first of the pair of p-channel MOS transistors; and

providing biasing means for providing a biasing current to the voltage-controlled oscillator circuit and for substantially widening the tuning range thereof, the biasing means being configured according to a biasing n-channel MOS transistor connected to the supply voltage and a ~~biasing~~ self-biasing p-channel MOS transistor connected to the reference voltage,

wherein the biasing means is connected to the pair of p-channel MOS transistors and the at least one inductor.

20. (Currently amended) The method as in claim 19, the biasing p-channel MOS transistor having source, drain and gate terminals and the drain terminal of the biasing p-channel MOS transistor is connected to the reference voltage, further comprising the step of connecting the gate and drain terminals of the biasing p-channel MOS transistor.

21. (New) The method as in claim 19, the biasing n-channel MOS transistor having source, drain and gate terminals and the drain terminal of the biasing n-channel MOS transistor is connected to the supply voltage, further comprising the

step of connecting the gate terminal of the biasing n-channel MOS transistor to a biasing voltage.

22. (New) The method as in claim 19, further comprising the step of connecting the source terminal of the biasing n-channel MOS transistor to the source terminals of the pair of p-channel MOS transistors.

23. (New) The method as in claim 19, further comprising the step of configuring the at least one inductor according to a pair of first and second inductors connected in series.

24. (New) The method as in claim 23, further comprising the step of connecting the source terminal of the biasing p-channel MOS transistor to the inter-connection between the pair of first and second inductors.